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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/694,873	10/28/2003	John G. Heston	004578.1377	4101

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EXAMINER	
SANDVIK, BENJAMIN P	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 09/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/694,873	HESTON, JOHN G.	
	Examiner	Art Unit	
	Ben P. Sandvik	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election with traverse of group 1 in the reply filed on 7/15/2005 is acknowledged. The traversal is on the ground(s) that the election requirement is incorrect. This argument is found persuasive. The examiner has made a full examination of claims 1-24 in this action.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 are rejected under 35 U.S.C. 102(b) as being anticipated by Hatada (U.S. Patent #4693770).

With respect to **claim 1**, Hatada teaches a circuit having first (Fig. 2, 24), second (Fig. 2, 22), and third circuit portions (Fig. 2, 16), said first and third circuit portions each including at least one semiconductor circuit component (Col 3 Ln 28 and Col 3 Ln 35), and said second circuit portion including at least one non-semiconductor circuit component and being free of semiconductor circuit components (Col 3 Ln 25, "Al electrodes"), said second circuit portion having first

and second electrically conductive parts (Fig. 2, 22, for example the leftmost two electrodes), and said third circuit portion having third and fourth electrically conductive parts which are respectively coupled to said first and second electrically conductive parts (Fig. 2, 12, for example the leftmost two electrodes) by respective thermo-formed bonds (Col 3 Ln 55, "slight heating"); a first substrate with said first and second circuit portions disposed adjacent one side thereof (Fig. 2, 24), said first substrate having a semiconductor portion which has each said semiconductor circuit component of said first circuit portion therein (Fig. 2, 24); and a second substrate with said third circuit portion disposed adjacent one side thereof (Fig. 2, 16), said second substrate being physically separate from said first substrate and being oriented so that said one side thereof faces said one side of said first substrate (Fig. 2, 16 is separated from 24 by bumps), and said second substrate having a semiconductor portion which has each said semiconductor circuit component of said third circuit portion therein.

With respect to **claim 2**, Hatada teaches that said first circuit portion has one said circuit component thereof which is implemented in a first semiconductor technology, and that said third circuit portion has one said circuit component thereof which is implement in a second semiconductor technology different from said first semiconductor technology (Col 4 Ln 32-40, implies that one circuit is laser or LED and other circuit is a drive circuit).

With respect to **claim 6**, Hatada teaches thermocompression bonds (Col 51-58 and Claim 12).

With respect to **claim 7**, Hatada teaches that said first and second electrically conductive parts are each a contact (Fig. 2, 12), and that said third and forth electrically conductive parts are each a bump (Fig. 2, 14).

With respect to **claim 8**, Hatada teaches that each of said electrically conductive parts is made of gold (Col 3 Ln 20 and Col 4 Ln 12-13).

With respect to **claim 10**, Hatada teaches that said third circuit portion has therein a single said circuit component (Col 4 Ln 35, LED is a single circuit component).

With respect to **claim 12**, Hatada teaches that said first substrate is a semiconductor substrate (Col 4 Ln 8-12).

With respect to **claim 13**, Hatada teaches that said first substrate includes gallium arsenide, and that said second substrate includes gallium arsenide (Col 4 Ln 8-12).

With respect to **claim 15**, Hatada teaches providing a first semiconductor portion (Fig. 2, 24); forming first and second circuit portions adjacent one side of said first substrate (Fig. 2, 22), said first circuit portion including at least one semiconductor circuit component (Col 3 Ln 28), and said second circuit portion including at least one non-semiconductor circuit component and being free semiconductor circuit components (Col 3 Ln 25, "Al electrodes"), said second circuit portion having first and second electrically conductive parts (Fig. 2, 22, for example the leftmost two electrodes), and said semiconductor portion of said first

substrate having therein each said semiconductor circuit component of said first circuit portion (Fig. 2, 24); providing a second substrate which is physically separate from said first substrate and which has semiconductor portion and forming a third circuit portion adjacent one side of said second substrate (Fig. 2, 16), said third circuit portion including at least one semiconductor circuit component (Col 3 Ln 35), said third circuit portion having third and fourth electrically conductive parts (Fig. 2, 12, for example the leftmost two electrodes), and said semiconductor portion of said second substrate having therein each said semiconductor circuit component of said third circuit portion (Fig. 2, 16); orienting said second substrate relative to said first substrate so that said one side thereof faces said one side of said first substrate and said first and second electrically conductive parts are respectively engaging said third and fourth electrically conductive parts (Fig. 2, 12); creating a thermo-formed bond between said first and third electrically conductive parts and a further thermo- formed bond between said second and fourth electrically conductive parts, said first, second and third circuit portions being respective portions of a single circuit (Col 3 Ln 55, "slight heating").

With respect to **claim 16**, Hatada teaches that said forming of said first circuit portion includes implementing one said circuit component thereof in a first semiconductor technology; and wherein said forming of said third circuit portion includes implementing one said circuit component thereof in a second semiconductor technology different from said first semiconductor technology (Col

4 Ln 32-40, implies that one circuit is laser or LED and other circuit is a drive circuit).

With respect to **claim 20**, Hatada teaches that the creating of said thermo-formed bonds is carried out in a manner so that each of said thermo-formed bonds is one of a thermosonic bond and a thermocompression bond (Col 51-58 and Claim 12).

With respect to **claim 23**, Hatada teaches that said first substrate is a semiconductor substrate (Col 4 Ln 8-12).

With respect to **claim 24**, Hatada teaches that said first substrate includes gallium arsenide, and that said second substrate includes gallium arsenide (Col 4 Ln 8-12).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hatada, in view of Yu et al (U.S. Patent #6100593).

With respect to **claims 3 and 17**, Hatada teaches all of the limitations of claims 1 and 15, respectively, and bonds that are thermo-formed, but does not teach that said circuit includes a fourth circuit portion which includes at least one semiconductor circuit component, said second circuit portion having fifth and sixth electrically conductive parts, and said fourth circuit portion having seventh and eight electrically conductive parts which are respectively coupled to said fifth and sixth electrically conductive parts by respective thermo-formed bonds; and including a third substrate with said fourth circuit portion disposed adjacent one side thereof, said third substrate being physically separate from said first and second substrates and being oriented so that said one side thereof faces said one side of said first substrate, and said third substrate having a semiconductor portion which has each said semiconductor circuit component of said fourth circuit portion therein. Yu teaches a package with a configuration of a first substrate having first circuit portion (Fig. 3, 108) and second circuit portions that are coupled to a fourth circuit portion (Fig. 3, 109), the fourth circuit portion being on a third substrate that is physically separate and has one side that faces one side of the first substrate (Fig. 3, 116). It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a fourth circuit portion on a third substrate to the package of Hatada as taught by Yu in order to give the circuit more functional capabilities.

Claims 4, 5, 18, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hatada and Yu, in view of Nishizawa (U.S. PG Pub #20010011766).

With respect to **claims 4, 5, 18, and 19**, Hatada and Yu teach all of the limitations of claims 3 and 17, respectively, and furthermore teach that the third circuit portion and fourth circuit portions are implement in semiconductor technologies, but do not teach that the third and fourth circuit portions are implement in different semiconductor technologies. Nishizawa teaches a package with three circuit portions that are all implemented in different semiconductor technologies (Fig. 6, 33 and Paragraph 112: "controller chip", and Fig. 6, 34a, 34b and Paragraph 112 and Paragraph 180, "the IC card may be the one mounting both nonvolatile memory and the volatile memory"). It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the third and fourth circuit portions of Hatada and Yu implemented in different semiconductor technologies as taught by Nishizawa in order to give the circuit more functional capabilities.

Claims 9 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hatada.

With respect to **claims 9 and 21**, Hatada does not explicitly state that said third circuit portion has one said circuit component thereof with a fabrication yield

which is lower than a fabrication yield of each said circuit component of said first circuit portion. However, Hatada teaches that the circuit portions can be different devices made from dissimilar materials (Col 4 Ln 32-40). It would have been obvious to one of ordinary skill in the art at the time the invention was made that the first and third circuit portions of Hatada have different fabrication yields and to provide the circuit with lower fabrication yield as the third circuit portion in order to increase the final yield of the finished package by fabricating the circuit portions separately and joining them later.

Furthermore, with respect to **claim 9**, note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Fitzgerald, 205 USPQ 594, 596 (CCPA); In re Marosi et al., 218 USPQ 289 (CAFC); and most recently, In re Thorpe et al., 227 USPQ 964 (CAFC, 1985) all of which make it clear that it is the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that Applicant has burden of proof in such cases as the above case law makes clear.

As to the grounds of rejection under section 103, see MPEP § 2113

Claims 11 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hatada, in view of Hoffman (U.S. Patent #6576998).

With respect to **claims 11 and 22**, Hatada teaches all of the limitations of claims 10 and 21, respectively, but does not teach that said single circuit component of said third circuit portion is a transistor. Hoffman teaches a package with multiple circuit portions wherein one of the portions is a single transistor (Fig. 1, 36 and Col 2 Ln 57). It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the third circuit portion of Hatada a single transistor as taught by Hoffman in order to use the circuit portion as a switch.

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hatada, in view of Sayagani et al (U.S. PG Pub #20020072147).

With respect to **claim 14**, Hatada teaches all of the limitations of claim 1, but does not teach that the circuit is a microwave circuit. Sayagani teaches a multi-chip package that is used as a high-frequency package (Fig. 1 and Paragraph 39). It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the package of Hatada a high-frequency package usably in microwave applications as taught by Sayagani in order to use the package as a high frequency signal processor.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ben P. Sandvik whose telephone number is (571) 272-8446. The examiner can normally be reached on Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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